Charge-Trapping Memory Device and Methods for Operating and Manufacturing the Cell

ABSTRACT OF THE DISCLOSURE

The charge-trapping layer comprises two strips above the source and drain junctions. The thicknesses of the charge-trapping layer and the gate dielectric are chosen to facilitate Fowler-Nordheim-tunnelling of electrons into the strips during an erasure process. Programming is performed by injection of hot holes into the strips individually for two-bit storage.